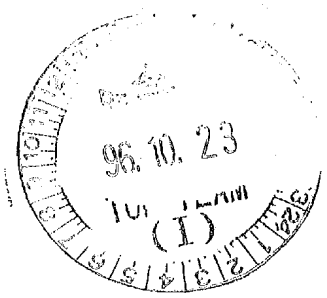
ELLA CHEONG | SPRUSON & FERGUSON
PATENT, DESIGN AND TRADE MARK AGENTS
SINGAPORE

OUR REF : 10677SG112/TSN
YOUR REF: 0503-A30328SG
DATE : 15 October 2007
FAX : 886 2 2755 2737
PAGES : 7

CONFIRMATION

Top Team International Patent & Trademark Office
3rd Floor, No. 279
Sec. 4, Hsin-Yi Rd
Taipei
Taiwan



Attn: Ms. Peggy Wu

Dear Peggy,

Singapore Patent Application No. 200403840-2
Invention: High-K Gate Dielectric Stack Plasma Treatment To Adjust Threshold Voltage Characteristics
Applicant: Taiwan Semiconductor Manufacturing Co., Ltd.

We write to report that the above-referenced application has undergone substantive examination by the **Austrian Patent Office** on behalf of the Intellectual Property Office of Singapore (IPOS).

We enclose a Written Opinion for your attention and comments and a response to the Written Opinion is due by **21 February 2008** (no extension is available).

The Examination was based on the application as **originally filed.**

The Examiner has deemed that Claims 1-20 possess novelty, but do not involve an inventive step in view of the cited documents, D1: US2002/0175393 and D2: US 5,281, 546 mentioned in the Written Opinion.

The report is self-explanatory and the reasons for the above observations are stated in pages 1 and 2 of the Written Opinion. We would be grateful if you could provide us comments on the objections.

Please note that any response must be filed in Singapore and the deadline for replying, **21 February 2008** is inextensible. If no response is filed by that date, the application will not be refused. However, it would mean the end of the examination procedure and the final Examination Report would contain the same comments as in the enclosed Written Opinion. The application would also be granted on the basis of the current specification, unless voluntary amendments were submitted before grant. Any such voluntary amendments would not be examined.

EC|SF
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If no response is to be filed, we would appreciate knowing that as soon as it is decided, so that we do not send you any unnecessary reminders.

Please do not hesitate to contact us if you have any queries.

Yours faithfully,

Alex Tan
ELLA CHEONG SPRUSON & FERGUSON (SINGAPORE)
Encl

IPOS

Intellectual Property Office of Singapore
51 Bras Basah Road #04-01
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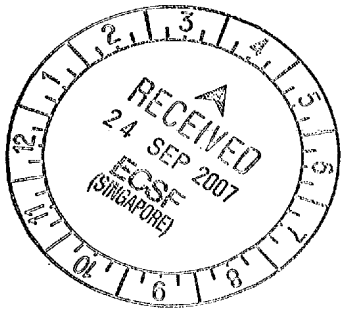
RF 240

In Reply Please Quote Our Reference TSN

Your Ref	:	10677SG112/TSN/SNG
Our Ref	:	2004038402/070921/TMMHO/0567
Date	:	21/09/2007
Writer's Direct Line	:	63302748



ELLA CHEONG SPRUSON & FERGUSON (SINGAPORE) PTE LTD
P.O. BOX 1531
ROBINSON ROAD POST OFFICE
SINGAPORE 903031

Dear Sir,

Singapore Patent Application No.: 200403840-2
Title of invention: HIGH-K GATE DIELECTRIC STACK PLASMA TREATMENT TO ADJUST THRESHOLD VOLTAGE CHARACTERISTICS
Applicant(s): TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD. (TW)

INVITATION TO RESPOND TO WRITTEN OPINION

We forward with this letter a copy of the Written Opinion drawn up by the Examiner in connection with your request for an Examination Report.

You are invited to respond to the opinion by submitting:

(a) Written submissions or arguments disagreeing with the Examiner's opinion and/or
(b) An amendment of the specification of the application.

If you intend to respond, the response must be filed within 5 months from the date of this letter. You are also advised to inform us early if you do not intend to respond.

The Examiner will proceed to establish the Examination Report if no response is received by the end of the prescribed period.

If you have any further queries, please do not hesitate to contact the undersigned.

Thank you.

Yours faithfully,

Muhammad Haramain Osman
for REGISTRAR OF PATENTS
SINGAPORE

Austrian Patent Office
Service and Information Center
(TRF)

Dresdner Straße 87
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To

INTELLECTUAL PROPERTY OFFICE OF SINGAPORE
51 Bras Basah Road #04-01
Plaza By The Park

SINGAPORE 189554

Date of mailing: 13. Aug. 2007

Applicant
TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.

Application No.	Filing Date	(Earliest) Priority Date
200403840-2	**10 June 2004 (10.06.2004)**	**1 October 2003 (01.10.2003)**

International Patent Classification (IPC[8])
H01L 21/28 (2006.01); *H01L 21/316* (2006.01); *H01L 21/336* (2006.01); *H01L 29/78* (2006.01)

Please find enclosed the

☐ **SEARCH REPORT**

☐ **EXAMINATION REPORT**

☒ **WRITTEN OPINION**

provided by the Austrian Patent Office as Search and Examination Authority according to the Memorandum of Understanding between the Government of Singapore and the Austrian Patent Office (MOU)

Best regards

AUSTRIAN PATENT OFFICE Service and Information Center TRF	Dr. Koller

Enclosures:

☐ the search report
(it is also accompanied by a copy of each prior art document cited in the report)

☐ the examination report

☒ the written opinion

☐ the Registry's copy of the priority application

Austrian Patent Office

Application No.	Applicant:
200403840-2	TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.
Filing date	(Earliest) Priority Date
10 June 2004 (10.06.2004)	1 October 2003 (01.10.2003)

GENERAL OBSERVATIONS

☒ Unity of invention is given.
Consequently, all parts of the application were the subject of examination in establishing this report.

☒ Basis of the opinion:
The written opinion has been drawn on the basis of the application as transmitted with the request; and in consideration of the search report prepared by the US Patent Office, dated 28.11.2005.

☒ This report has been established in consideration of the claimed priority dated 01.10.2003.
Thus for the purposes of this report, the filing date indicated above is considered to be the relevant priority date.

☒ Further Remarks:
Concerning the search report and the written opinion the following general remarks are made:
Application of search report of USPTO is limited because priority date needs to be considered. Patent number of US 5281546 is cited erroneously (US 5282546 is noted, which is a patent that is not related to the topic of the application).

☒ The Applicant is thereby INVITED TO REPLY to this opinion within 5 months from the date of the Registrar's letter enclosing the written opinion.
HOW? By submitting a written reply, accompanied where appropriate, by the amendments.
IF NO REPLY IS TRANSMITTED, the examination report will be established on the basis of this written opinion.
The Applicant's attention is drawn to the fact that a later submission will be considered not to have been made and will therefore not be taken into account.

AUSTRIAN PATENT OFFICE Dresdner Straße 87, A-1200 VIENNA Facsimile No. ++431/53424/535	Authorized Officer **Kárpáty** Telephone No. ++431/53424

☐ EXAMINATION REPORT
☒ WRITTEN OPINION

Application No.
200403840-2

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Date of actual completion of the report / opinion: **27 June 2007 (27.06.2007)**

1. STATEMENT

Novelty (N)	YES	Claims	1-20
	NO	Claims	----
Inventive step (IS)	YES	Claims	----
	NO	Claims	1-20
Industrial applicability (IA)	YES	Claims	1-20
	NO	Claims	----

2. CITATIONS AND EXPLANATIONS

Reference is made to the following documents cited in the search report:

D1: US 2002/0175393 A1
D2: US 5281546 A

Documents US 6803275 B1 (12.10.2004) and US 2004/0152304 A1 (05.08.2004) were published after the priority date and the filing date. These documents are not considered for the purpose of this report.

Document US 6740605 B1 (25.05.2004) was published after the priority date and before the filing date and is not considered for the purpose of this report.

Present application discloses a method for treating a gate structure comprising a high-K gate dielectric stack to improve electric performance characteristics including providing a gate dielectric layer stack including a binary oxide over a silicon substrate; forming a polysilicon layer over the gate dielectric layer stack; lithographically patterning and etching to form a gate structure; and, carrying out at least one plasma treatment of the gate structure comprising a plasma source gas selected from the group consisting of H_2, N_2, O_2, and NH_3.

D1 displays source reagent compositions for CVD formation of gate dielectric thin films using amide precursors and methods of using the same.

D2 shows a method of fabricating a thin film transistor using hydrogen plasma treatment of the intrinsic silicon/doped layer interface. D2 describes that hydrogen plasma treatment improves electrical characteristics of amorphous silicon layer.

Novelty:

Claims 1, 13 meet requirements of novelty because none of the cited documents teaches all the features of these claims.

Dependent claims 2-12 and 14-20 add additional features to claims 1 and 13, therefore they are also new.

Inventive Step:

Claims 1, 13 do not meet requirements of inventive step for the following reason:
The following were obvious to a skilled professional well-informed as to the state of the art at the time of the priority date:
- providing a gate dielectric layer stack comprising a binary oxide over a silicon substrate:
Formation of SiO_2 as gate insulator is part of the commonly known MOSFET fabrication process steps.
- forming a polysilicon layer over the gate dielectric layer stack
Poly-Si is commonly used material in the microelectronic industry; poly-Si is particularly common as Gate electrode.
- lithographically patterning and etching to form a gate structure
Lithography, Wet Etch or Reactive Ion Etch are commonly used processes in the microelectronic industry.
- carrying out at least one plasma treatment of the gate structure comprising a plasma source gas selected from the group consisting of H_2, N_2, O_2, and NH_3
D2 clearly states that "improved electrical performance results from fewer defects along the interface of poly-Si as a consequence of both the physical and chemical interactions of the hydrogen plasma with the intrinsic silicon in which impurities are removed from the surface" (C2, R26-30). For one who is skilled in the art it is obvious that hydrogen plasma is usable for inner surface interfaces (poly-Si – HfO_2) as well.
-annealing the gate structure following the at least one plasma treatment

Claims 2, 3, 4, 14, 15 do not meet requirements of inventive step for the following reason:
Annealing step is widely used in the semiconductor industry for reducing stress, to minimize crystalline defects, and reducing dangling bonds of poly-Si.

Claims 5, 16 do not meet requirements of inventive step for the following reason:
Formation of SiO_2 as gate insulator is part of the commonly known MOSFET fabrication process steps.

Claims 6, 7, 8, 17, 18 do not meet requirements of inventive step for the following reason:
D1 describes listed materials as a result of using method of depositing layers described in D1. Repeated step(s) of depositing additional layer(s) of listed materials cannot be regarded as constituting inventive step.

Claims 9, 10, 11, 12, 19, 20 do not meet requirements of inventive step for the following reason:
D2 clearly states that "improved electrical performance results from fewer defects along the interface of poly-Si as a consequence of both the physical and chemical interactions of the hydrogen plasma with the intrinsic silicon in which impurities are removed from the surface" (C2, R26-30). For one who is skilled in the art it is obvious that hydrogen plasma is usable for inner surface interfaces (poly-Si – HfO_2) as well.

The present application's claims 1-20 do not show an inventive step over the pertintent state of the art.

Industrial application:

Industrial applicability is obvious.